

FIG. 1

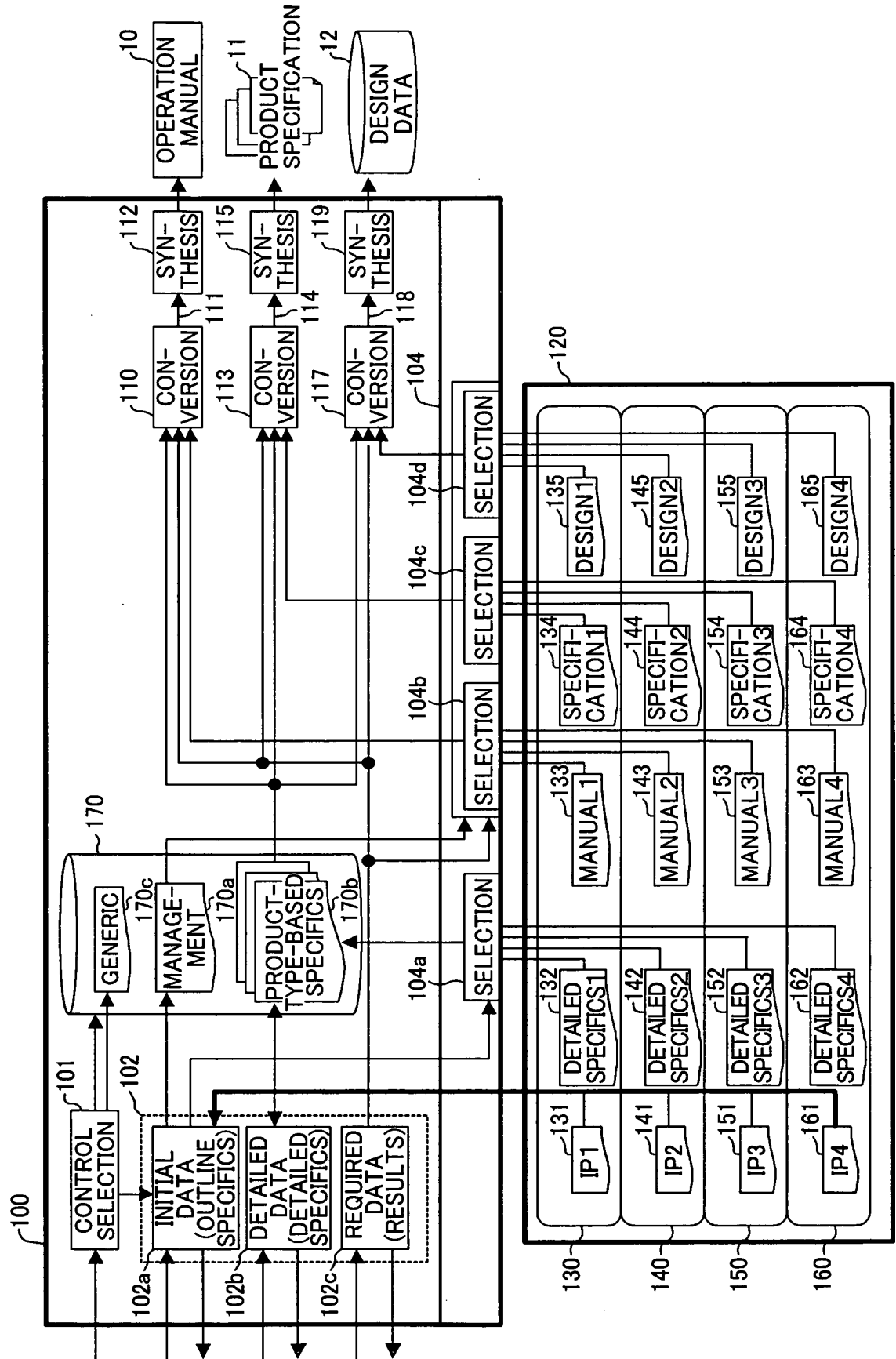


FIG. 2

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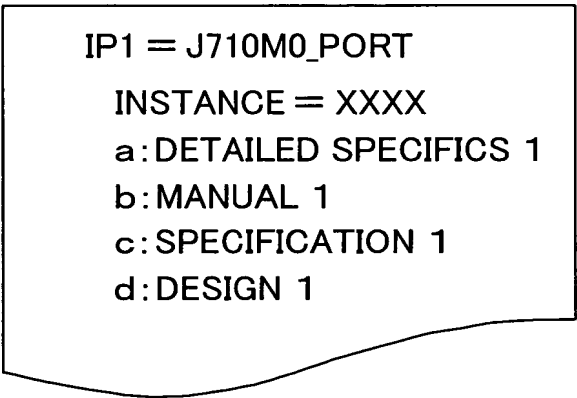


FIG. 3

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PORTn	PnOUT	PnIN	PnDIR	PnPLU
	ADDRESS	ADDRESS	ADDRESS	ADDRESS
	MSB...LSB	MSB...LSB	MSB...LSB	MSB...LSB
0				
1				

FIG. 4

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REGISTER NAME	DESCRIPTIONS (WITH P _n DIR)	DESCRIPTIONS (WITHOUT P _n DIR)
P _n OUT	TO OUTPUT DATA TO A TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P _n DIR) FOR THE PORT _n TO 1 AND WRITE THE DATA ON THE OUTPUT REGISTER (P _n OUT) FOR THE PORT _n .	TO OUTPUT DATA TO A TERMINAL, WRITE THE DATA ON THE OUTPUT REGISTER (P _n OUT) FOR THE PORT _n .
P _n IN	TO READ THE DATA INPUTTED TO THE TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P _n DIR) FOR THE PORT _n TO 0 AND READ OUT THE VALUE OF THE INPUT REGISTER (P _n IN) FOR THE PORT _n .	TO READ THE DATA INPUTTED TO THE TERMINAL, READ OUT THE VALUE OF THE INPUT REGISTER (P _n IN) FOR THE PORT _n .
P _n DIR	IN THE PORT _n , INPUT/OUTPUT DIRECTIONS CAN BE CONTROLLED ON A BIT-BY-BIT BASIS BY THE DIRECTION CONTROL REGISTER (P _n DIR) FOR THE PORT _n . WHEN THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P _n DIR) FOR THE PORT _n INDICATES 1, AN OUTPUT MODE RESULTS, AND WHEN THE CONTROL FLAG INDICATES 0, AN INPUT MODE RESULTS.	-
P _n PLU	IN THE PORT _n , PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL REGISTER (P _n PLU) FOR THE PORT _n . WHEN THE CONTROL FLAG OF THE PULL-UP RESISTOR CONTROL REGISTER (P _n PLU) OF THE PORT _n IS SET TO 1, A PULL-UP RESISTOR IS ADDED.	=

FIG. 5

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P_{nm}

INPUT VOLTAGE HIGH LEVEL	V _{IH}		0.8V _{DD}		V _{DD}	V
INPUT VOLTAGE LOW LEVEL	V _{IL}		V _{SS}		0.2V _{DD}	
PULL-UP RESISTOR	R _{IH}	WITH PULL-UP RESISTOR V _{IN} = 1.2 V	36	90	180	kΩ
INPUT LEAKAGE CURRENT	I _{LI}	WITHOUT PULL-UP RESISTOR V _{IN} = 0 ~ V _{DD}			±2	μA
OUTPUT VOLTAGE HIGH LEVEL	V _{OH}	I _{OH} = -300 μA	2.4			
OUTPUT VOLTAGE LOW LEVEL	V _{OL}	I _{OL} = 1.6 mA			0.6	V

FIG. 6

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MODULE FROM WHICH WIRING STARTS			MODULE TO WHICH WIRING EXTENDS		
MODULE	INSTANCE	TERMINAL	MODULE	INSTANCE	TERMINAL
J710M0_PORT		p0out0			
			J710M0_PORT		p0in0
J710M0_PORT		p0dir0			
J710M0_PORT		p0plu0			
J710M0_PORT		p1out7			
			J710M0_PORT		p1in7
J710M0_PORT		p1dir7			
J710M0_PORT		p1plu7			

FIG. 7

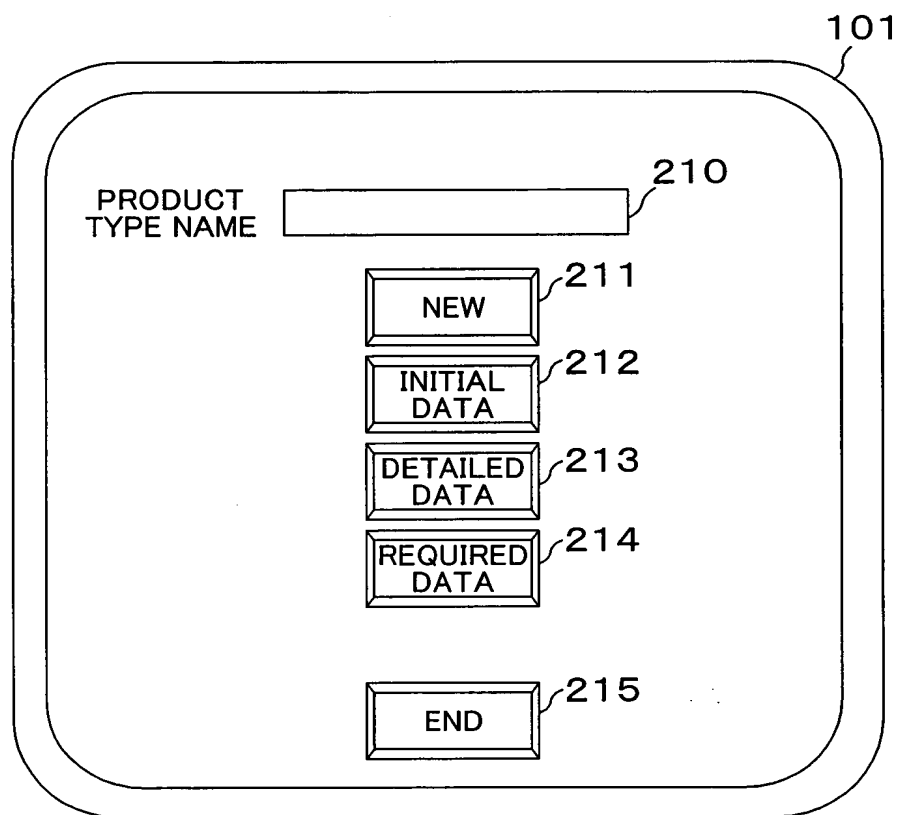


FIG. 8

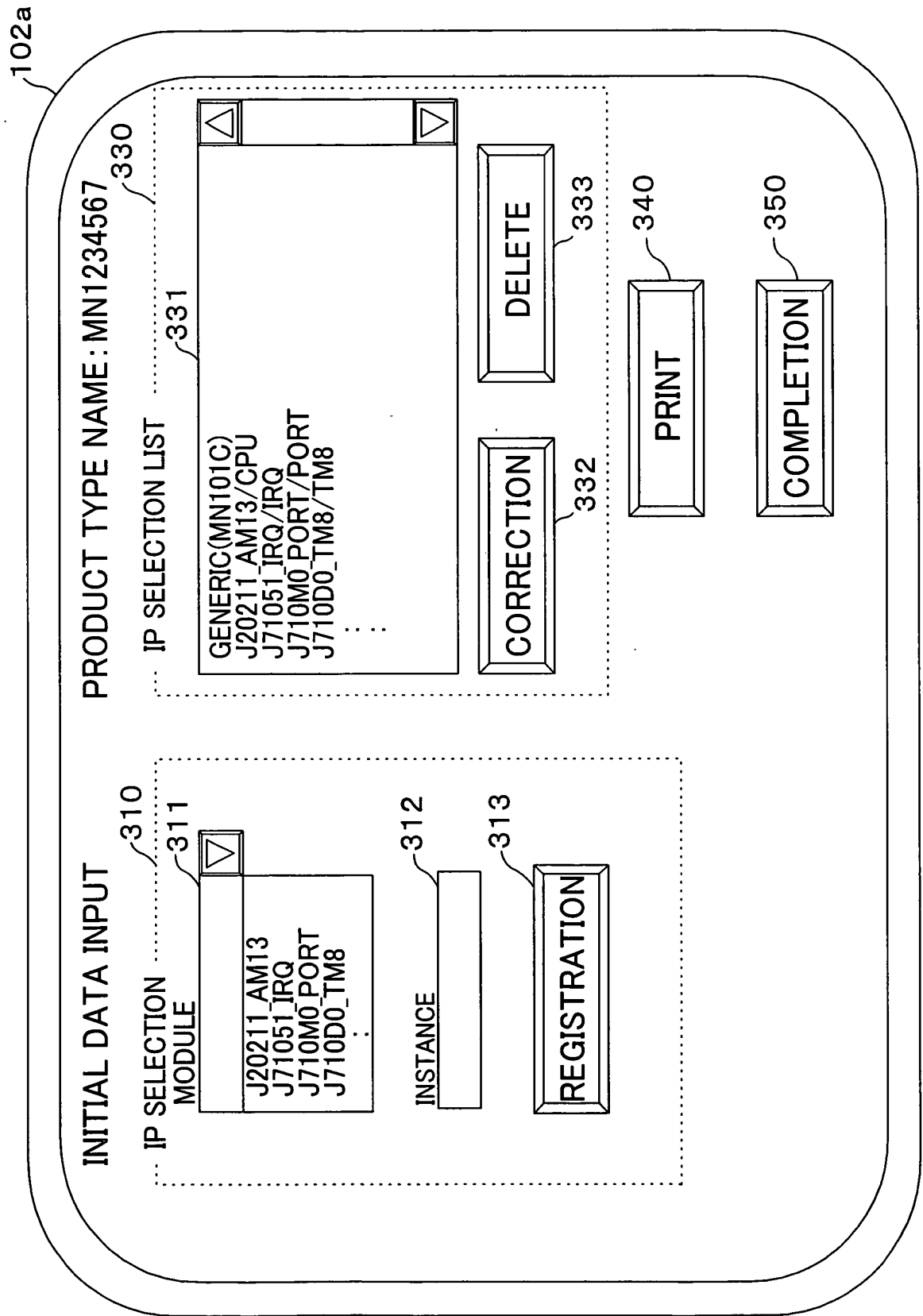


FIG. 9

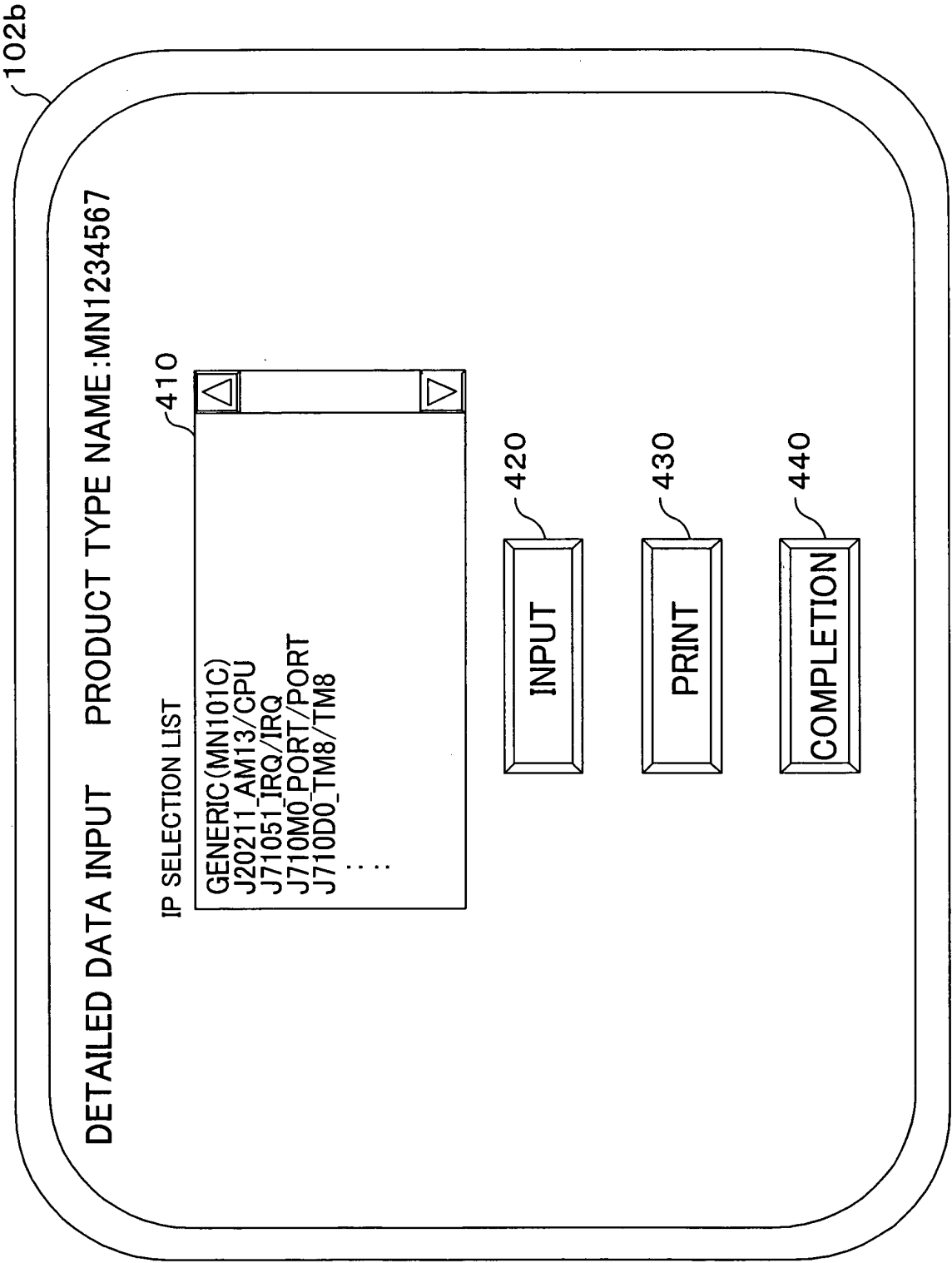


FIG. 10

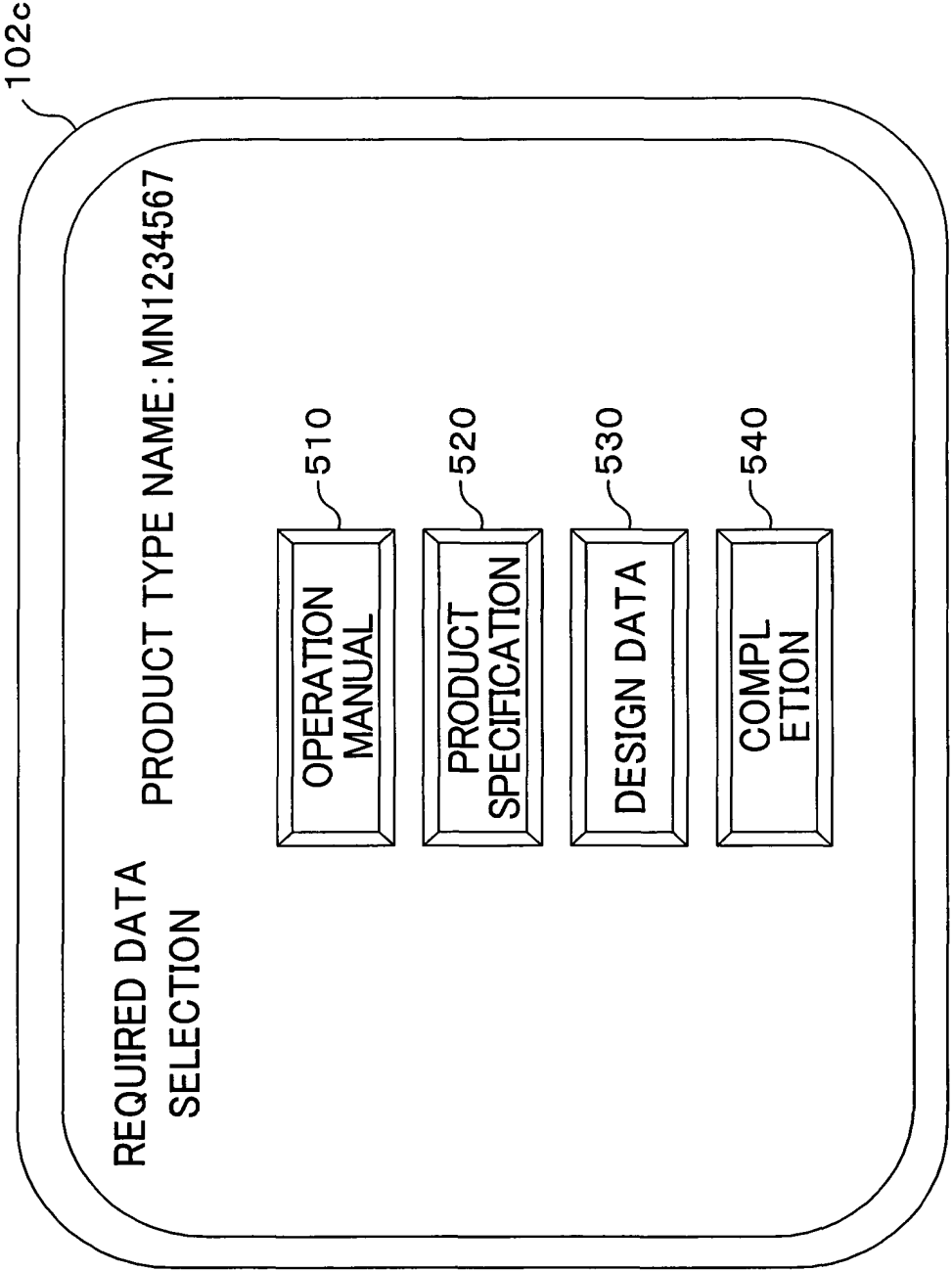


FIG. 11

170a

IP2=J20211_AM13
INSTANCE= CPU
a: DETAILED SPECIFICS 2
b: MANUAL 2
c: SPECIFICATION 2
d: DESIGN2

IP3=J71051_IRQ
INSTANCE= IRQ
a: DETAILED SPECIFICS3
b: MANUAL3
c: SPECIFICATION 3
d: DESIGN3

IP1=J710M0_PORT
INSTANCE= PORT
a: DETAILED SPECIFICS1
b: MANUAL1
c: SPECIFICATION 1
d: DESIGN1

IP4=J710D0_TM8
INSTANCE= TM8
a: DETAILED SPECIFICS4
b: MANUAL4
c: SPECIFICATION 4
d: DESIGN4

FIG. 12

170b

PORT _n	PnOUT	PnIN	PnDIR	PnPLU
	ADDRESS	ADDRESS	ADDRESS	ADDRESS
	MSB... LSB	MSB... LSB	MSB... LSB	MSB... LSB
0	3F10	3F20	3F30	3F40
	01111111	01111111	01111111	01111111
1	3F11	3F21	NOT	3F41
	00011111	00011111		00011111

FIG. 13

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<section><heading>DESCRIPTIONS FOR PORT 0 </heading>

<section position = "square">

<heading>SETTING OF GENERAL-PURPOSE PORT</heading>

<para>TO OUTPUT DATA TO A TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (PODIR) FOR THE PORT 0 TO 1 AND WRITE THE DATA ON THE OUTPUT REGISTER (POOUT) FOR THE PORT 0. </para>

<para>TO READ THE DATA INPUTTED TO THE TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (PODIR) FOR THE PORT 0 TO 0 AND READ OUT THE VALUE OF THE INPUT REGISTER (POIN) FOR THE PORT 0. </para>

<para>IN THE PORT 0, INPUT/OUTPUT DIRECTIONS CAN BE CONTROLLED ON A BIT-BY-BIT BASIS BY THE DIRECTION CONTROL REGISTER (PODIR) FOR THE PORT 0. WHEN THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (PODIR) FOR THE PORT 0 INDICATES 1, AN OUTPUT MODE RESULTS, AND WHEN THE CONTROL FLAG INDICATES 0, AN INPUT MODE RESULTS. </para>

<para>IN THE PORT 0, PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL REGISTER (POPLU) FOR THE PORT 0. WHEN THE CONTROL FLAG OF THE PULL-UP RESISTOR CONTROL REGISTER (POPLU) OF THE PORT 0 IS SET TO 1, A PULL-UP RESISTOR IS ADDED. </para>

</section> </section>

<section><heading>DESCRIPTIONS FOR PORT 1</heading>

<section position = "square">

<heading>SETTING OF GENERAL-PURPOSE PORT</heading>

<para>TO OUTPUT DATA TO A TERMINAL, WRITE THE DATA ON THE OUTPUT REGISTER (P1OUT) FOR THE PORT 1. </para>

<para>TO READ THE DATA INPUTTED TO THE TERMINAL, READ OUT THE VALUE OF THE INPUT REGISTER (P1IN) FOR THE PORT 1. </para>

<para>IN THE PORT 1, PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL REGISTER (P1PLU) FOR THE PORT 1. WHEN THE CONTROL FLAG OF THE PULL-UP RESISTOR CONTROL REGISTER (P1PLU) OF THE PORT 1 IS SET TO 1, A PULL-UP RESISTOR IS ADDED. </para>

</section></section>

FIG. 14

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P00

INPUT VOLTAGE HIGH LEVEL	V_{IH}		$0.8V_{DD}$	V_{DD}	V
INPUT VOLTAGE LOW LEVEL	V_{IL}		V_{SS}	$0.2V_{DD}$	
PULL-UP RESISTOR	R_{IH}	WITH PULL-UP RESISTOR $V_{IN} = 1.2 V$	36	180	$k\Omega$
INPUT LEAKAGE CURRENT	I_{LI}	WITHOUT PULL-UP RESISTOR $V_{IN} = 0 \sim V_{DD}$		± 2	μA
OUTPUT VOLTAGE HIGH LEVEL	V_{OH}	$I_{OH} = -300 \mu A$	2.4		V
OUTPUT VOLTAGE LOW LEVEL	V_{OL}	$I_{OL} = 1.6 mA$		0.6	

P01

INPUT VOLTAGE HIGH LEVEL	V_{IH}		$0.8V_{DD}$	V_{DD}	V
INPUT VOLTAGE LOW LEVEL	V_{IL}		V_{SS}	$0.2V_{DD}$	
PULL-UP RESISTOR	R_{IH}	WITH PULL-UP RESISTOR $V_{IN} = 1.2 V$	36	180	$k\Omega$
INPUT LEAKAGE CURRENT	I_{LI}	WITHOUT PULL-UP RESISTOR $V_{IN} = 0 \sim V_{DD}$		± 2	μA
OUTPUT VOLTAGE HIGH LEVEL	V_{OH}	$I_{OH} = -300 \mu A$	2.4		V
OUTPUT VOLTAGE LOW LEVEL	V_{OL}	$I_{OL} = 1.6 mA$		0.6	

FIG. 15

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MODULE FROM WHICH WIRING STARTS			MODULE TO WHICH WIRING EXTENDS		
MODULE	INSTANCE	TERMINAL	MODULE	INSTANCE	TERMINAL
J710M0_PORT	PORT	p0out0	iobuf	p00io	out
iobuf	p00io	in	J710M0_PORT	PORT	p0in0
J710M0_PORT	PORT	p0dir0	iobuf	p00io	dir
J710M0_PORT	PORT	p0plu0	iobuf	p00io	plu
J710M0_PORT	PORT	p1out7	open	open	open
iobuf	FIX	0	J710M0_PORT	PORT	p1in7
J710M0_PORT	PORT	p1dir7	open	open	open
J710M0_PORT	PORT	p1plu7	open	open	open

FIG. 16

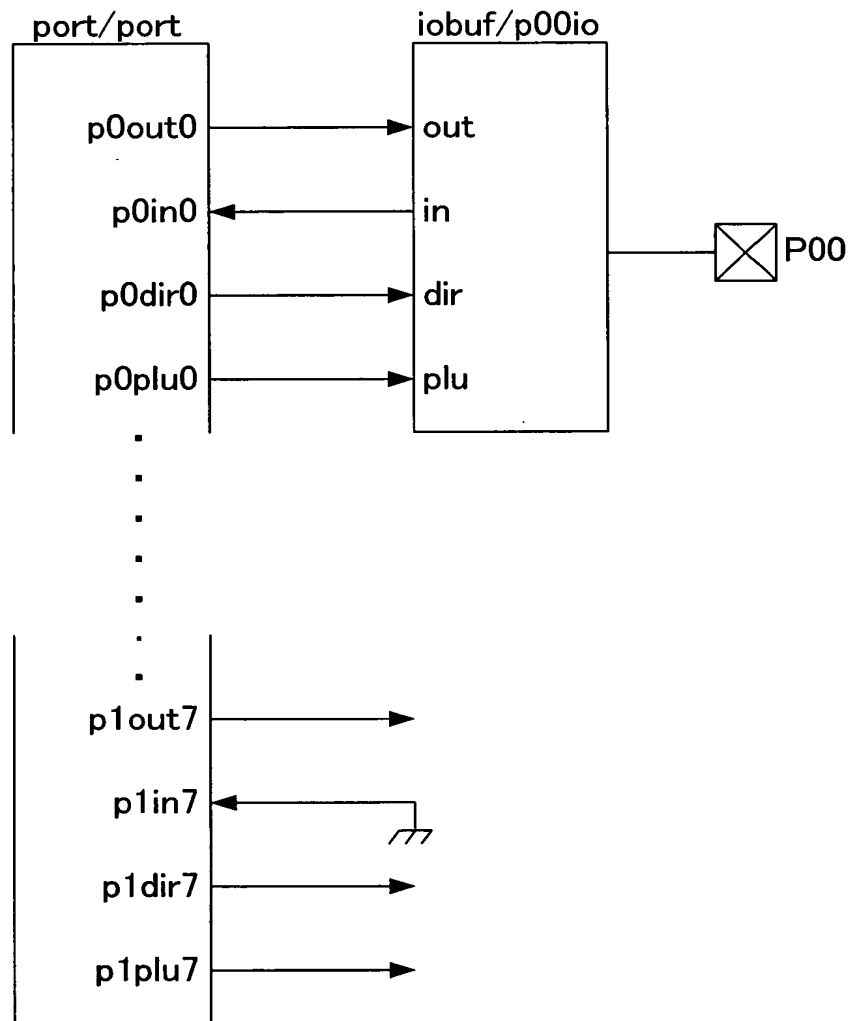


FIG. 17

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4.1 FUNCTIONS OF PORT 0

4.1.1 DESCRIPTIONS FOR PORT 0

■ SETTING OF GENERAL-PURPOSE PORT

TO OUTPUT DATA TO A TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0 TO 1 AND WRITE THE DATA ON THE OUTPUT REGISTER (P0OUT) FOR THE PORT 0.

TO READ THE DATA INPUTTED TO THE TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0 TO 0 AND READ OUT THE VALUE OF THE INPUT REGISTER (P0IN) FOR THE PORT 0.

IN THE PORT 0, INPUT/OUTPUT DIRECTIONS CAN BE CONTROLLED ON A BIT-BY-BIT BASIS BY THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0. WHEN THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0 INDICATES 1, AN OUTPUT MODE RESULTS, AND WHEN THE CONTROL FLAG INDICATES 0, AN INPUT MODE RESULTS.

IN THE PORT 0, PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL REGISTER (P0PLU) FOR THE PORT 0. WHEN THE CONTROL FLAG OF THE PULL-UP RESISTOR CONTROL REGISTER (P0PLU) OF THE PORT 0 IS SET TO 1, A PULL-UP RESISTOR IS ADDED.

FIG. 18

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		PRODUCT SPECIFICATION		MN1234567	
		ALL PAGES IN SPECIFICATION		-	PAGE 10
C. ELECTRIC CHARACTERISTICS					
Ta=-40°C~+85°C VDD=3 V VSS=0 V					
P00					
ITEM	ABBREVIATION	CONDITION	ALLOWABLE VALUE		UNIT
			MIN-IMUM	STANDARD-ARD	
INPUT VOLTAGE HIGH LEVEL	V _{IH}		0.8V _{DD}		V
INPUT VOLTAGE LOW LEVEL	V _{IL}		V _{SS}	0.2V _{DD}	
PULL-UP RESISTOR	R _{IH}	WITH PULL-UP RESISTOR V _{IN} = 1.2 V	36	90	kΩ
INPUT LEAKAGE CURRENT	I _{LI}	WITHOUT PULL-UP RESISTOR V _{IN} = 0~V _{DD}			μA
OUTPUT VOLTAGE HIGH LEVEL	V _{OH}	I _{OH} = -300 μA	2.4		
OUTPUT VOLTAGE LOW LEVEL	V _{OL}	I _{OL} = 1.6 mA		0.6	V

FIG. 19

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```

module SAMPLE (
P00,
.
.
.
P17);

input    P00;
.
.
input    P17;

wire     p00io_in_net0;
.
.
.
wire     p17io_in_net7;
wire     PORT_p0dir0_net8;
wire     PORT_p0out0_net9;
wire     PORT_p0plu0_net10;
.
.
.
wire     PORT_p1dir7_net53;
wire     PORT_p1out7_net54;
wire     PORT_p1plu7_net55;

iobuf p00io (
. io(P00),
. in(p00io_in_net0),
. dir(PORT_p0dir0_net8),
. out(PORT_p0out0_net9),
. plu(PORT_p0plu0_net10));
.
.
.

```

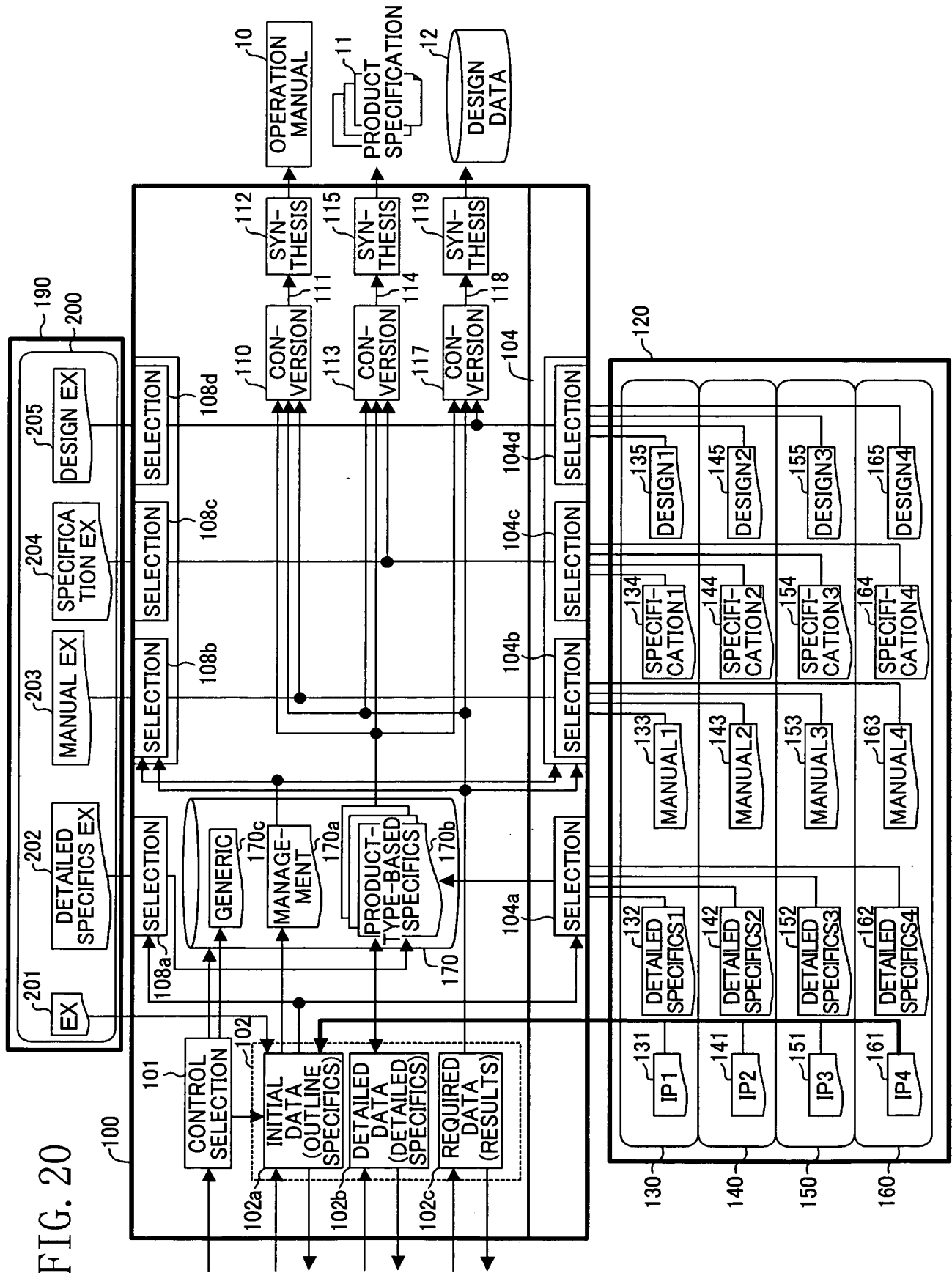


FIG. 21

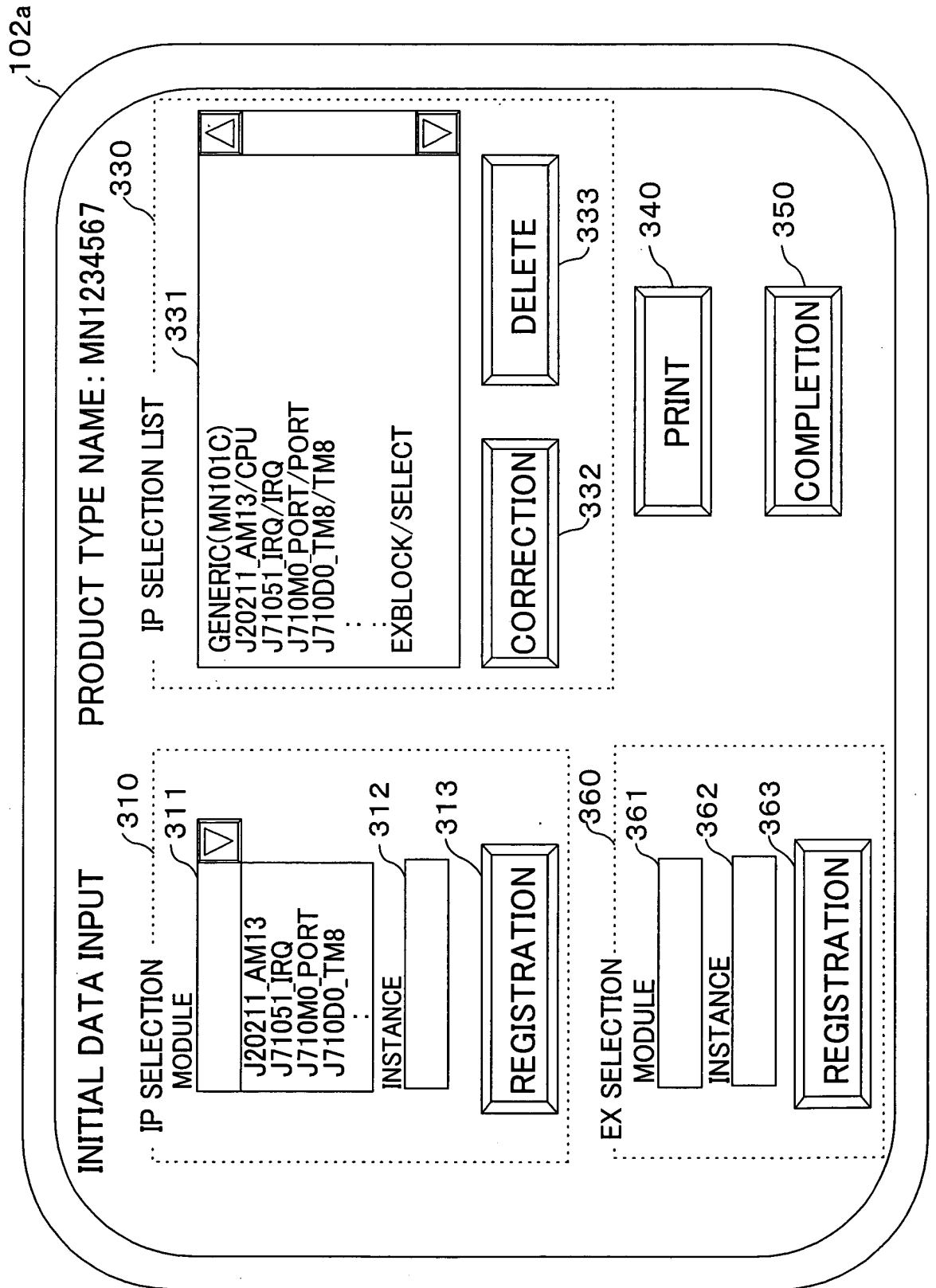


FIG. 23

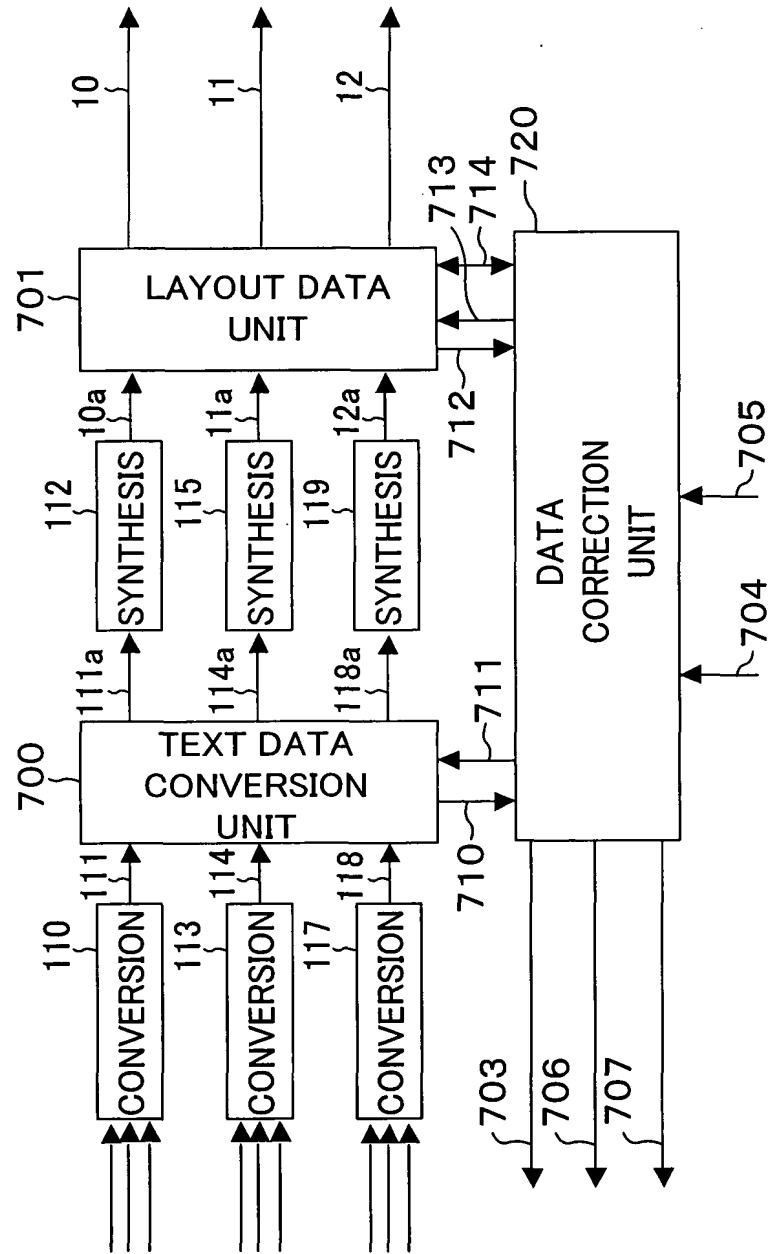
702

FIG. 24

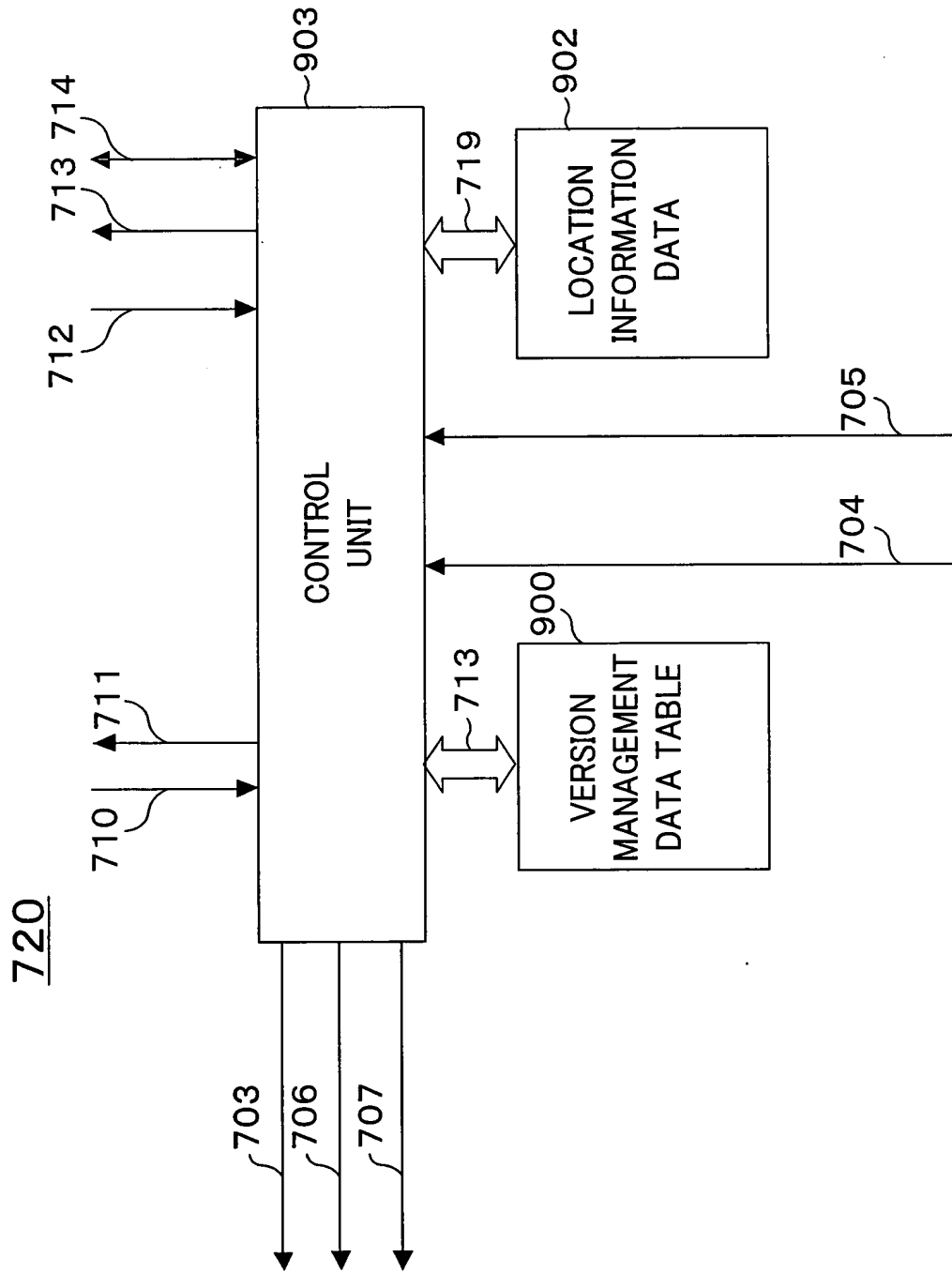


FIG. 25

900

IP MANAGEMENT DATA	VERSION
IP1	Ver 1
IP2	Ver 2
IP3	Ver 2
IP4	Ver 3

FIG. 26

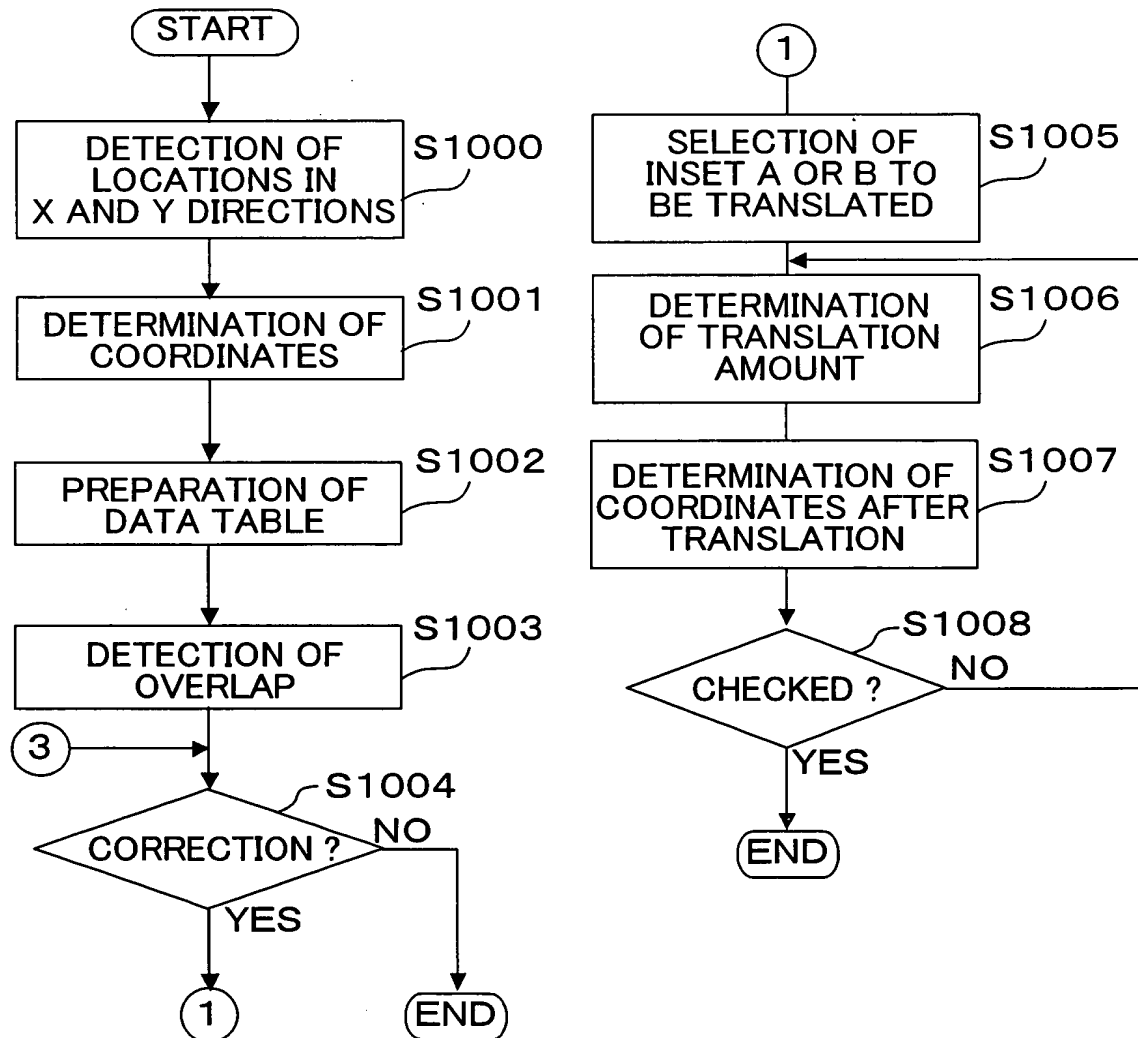


FIG. 27

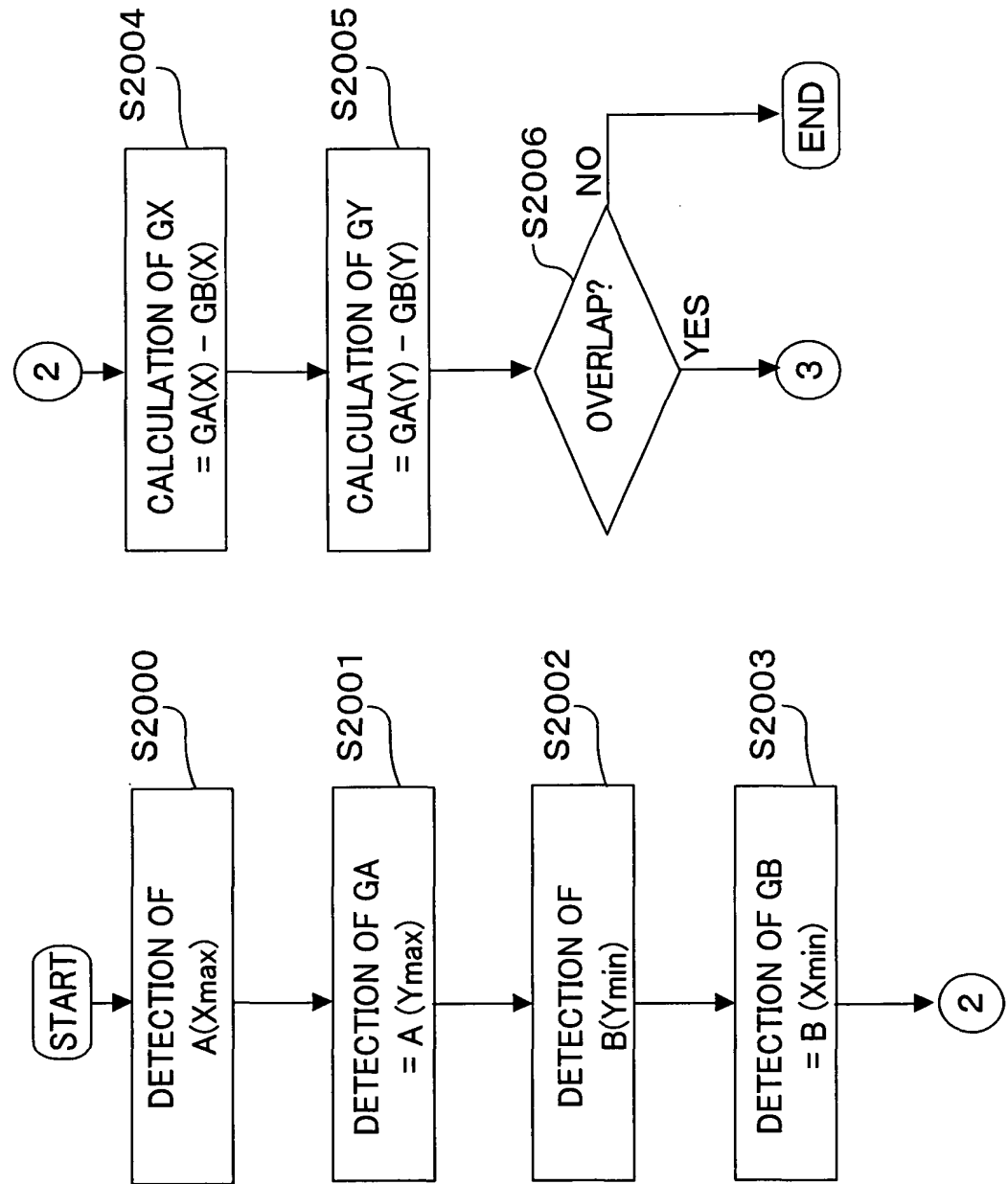


FIG. 28

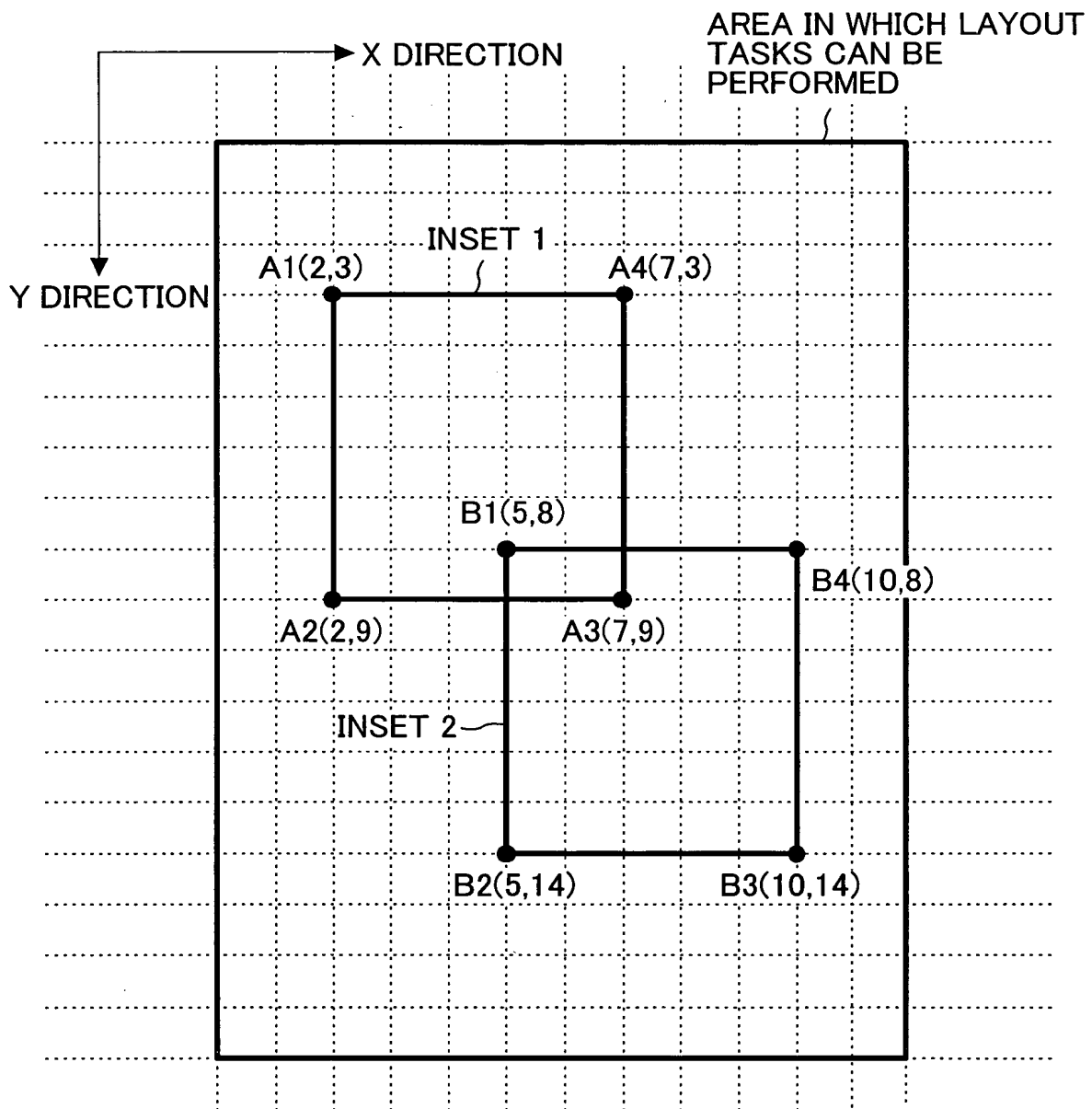
714 BEFORE CORRECTIONS

FIG. 29

902 BEFORE CORRECTIONS

	LOCATION INFOR- MATION1	LOCATION INFOR- MATION2	LOCATION INFOR- MATION3	LOCATION INFOR- MATION4
INSET 1	A1 (2, 3)	A2 (2, 9)	A3 (7, 9)	A4 (7, 3)
INSET 2	B1 (5, 8)	B2 (5, 14)	B3 (10, 14)	B4 (10, 8)

FIG. 30

902 AFTER CORRECTIONS

	LOCATION INFOR- MATION1	LOCATION INFOR- MATION2	LOCATION INFOR- MATION3	LOCATION INFOR- MATION4
INSET 1	A1 (2, 3)	A2 (2, 9)	A3 (7, 9)	A4 (7, 3)
INSET 2	B1 (5, 11)	B2 (5, 17)	B3 (10, 17)	B4 (10, 11)

FIG. 31

714 AFTER CORRECTIONS